AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS

1. (Currently Amended) A method for testing a circuit including AC coupled interconnects, the circuit ~~of a circuit~~ having a transmitting IC and a receiving IC that are coupled together by an AC interconnection, each IC having a Boundary Scan Cell (BSC) connected to a reference clock ~~and a source of an input signal~~, the method comprising:

generating an AC signal based on the reference clock and a value held in ~~of~~ the BSC of the transmitting IC ~~and the reference clock~~, the AC signal having a first phase if a first value is held in the BSC, and a second phase if a second value is held in the BSC;

generating, for the receiving IC, ~~transmitting~~ a sync pulse signal based on a test reset signal ~~to the BSC of the receiving IC;~~

capturing, in the BSC of the receiving IC, a default phase of said AC signal in response ~~relation~~ to said sync pulse signal;

sampling ~~capturing~~ a phase of the AC ~~input~~ signal;

comparing the default phase with the sampled ~~of the input signal with the~~ phase of the ~~said~~ AC signal ~~in relation to said sync pulse signal~~; and

generating a phase decode ~~sending an output~~ signal based on said comparing.

2. (Currently Amended) The method according to claim 1, wherein said generating an AC signal ~~further~~ comprises:

resetting the BSC of the transmitting IC.

3. (Currently Amended) The method according to claim 2, wherein said resetting ~~further~~ comprises:

latching a default value ~~generating a zero value signal~~ in a boundary scan register in the BSC of the transmitting IC.

4-7. (Cancelled)

8. (Currently Amended) A system for testing a circuit including AC coupled interconnects, the circuit ~~of a circuit~~ having a transmitting ~~driving~~ IC and a receiving IC that are coupled together by an AC interconnection, each IC having a plurality of boundary scan cells (BSCs) connected to a reference clock, the system comprising:

means for generating an AC signal based on the reference clock and a value held in ~~of~~ the BSC of the transmitting IC ~~and the reference clock~~, the AC signal having a first phase if a first value is held in the BSC, and a second phase if a second value is held in the BSC;

means for generating ~~transmitting~~ a sync pulse signal based on a test reset signal ~~to the BSC of the receiving IC;~~

means for capturing, in the BSC of the receiving IC, a default phase of said AC signal in response ~~relation~~ to said sync pulse signal;

means for sampling ~~capturing~~ a phase of the AC ~~input~~ signal;

means for comparing the default phase with the sampled ~~of the input signal with the~~ phase of the ~~said~~ AC signal ~~in relation to said sync pulse signal~~; and

means for generating a phase decode ~~sending an output~~ signal based on said comparing.

9. (Currently Amended) The system ~~method~~ according to claim 8, wherein said means for generating an AC signal ~~further~~ comprises:

means for resetting the BSC of the transmitting IC.

10. (Currently Amended) The system ~~method~~ according to claim 9, wherein said means for resetting ~~further~~ comprises:

means for latching a default value ~~generating a zero value~~ ~~signal~~ in a boundary scan register in the BSC of the transmitting IC.

11-14. (Cancelled)

15. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions readable by the machine to perform a method for testing a circuit including AC coupled interconnects, the circuit ~~of a circuit~~ having a transmitting IC and a receiving IC that are coupled together by an AC interconnection, each IC having a Boundary Scan Cell (BSC) ~~one BSC~~ connected to a reference clock ~~and an input signal~~, the method comprising:

generating an AC signal based on the reference clock and a value held in ~~of~~ the BSC of the transmitting IC ~~and the reference clock~~, the AC signal having a first phase if a first value is held in the BSC, and a second phase if a second value is held in the BSC;

generating, for the receiving IC, ~~transmitting~~ a sync pulse signal based on a test reset signal ~~to the BSC of the receiving IC;~~

capturing, in the BSC of the receiving IC, a default phase of said AC signal in response ~~relation~~ to said sync pulse signal;

sampling ~~capturing~~ a phase of the AC ~~input~~ signal;

comparing the default phase with the sampled ~~of the input signal with the~~ phase of the ~~said~~ AC signal ~~in relation to said sync pulse signal~~; and

generating a phase decode ~~sending an output~~ signal based on said comparing.

16. (Currently Amended) The program storage device ~~method~~ according to claim 15, wherein said generating an AC signal ~~further~~ comprises:

resetting the BSC of the transmitting IC.

17. (Currently Amended) The program storage device ~~method~~ according to claim 16, wherein said resetting ~~further~~ comprises:

latching a default value ~~generating a zero value~~ ~~signal~~ in a boundary scan register in the BSC of the transmitting IC.

18-21. (Cancelled)

22. (Currently Amended) An output AC boundary scan cell (BSC), comprising:

a first flip-flop having a data input connected to a *bscanShiftIn* line, a clock input connected to a *clockBscanAc* line, a test reset input connected to a *testBscanAc* line, and an output connected to a *bscanShiftOut* line;

a second flip-flop having a data input connected to said output of said first flip-flop, an update input connected to a *updateBscanAc* line, and a second flip-flop output;

an XOR logic gate having a first input connected to a *refClk* line, ~~and~~ a second input connected to said second flip-flop output, and an XOR logic gate output, said XOR logic gate is adapted to output an AC signal, the AC signal having a first phase if a first value is held in said second flip-flop holds, the AC signal having a second phase if a second value is held in said second flip-flop; and

a multiplexer ~~multiplexor~~ having a first input connected to a *fromCore* line, a select input connected to ~~and~~ a *selectJtagOut* line, ~~and~~ a second input connected to said XOR logic gate output, and a multiplexor output, said multiplexer selectively outputting a signal from the second input if a mode signal on the *selctJtagOut* line indicates an AC JTAG mode.

23. (Currently Amended) An output AC boundary scan cell (BSC) for generating a signal, said output AC BSC ~~boundary scan cell~~ comprising:

a first flip-flop for receiving and capturing a shift-in test data ~~resetting the output AC boundary scan cell~~;

a second flip-flop connected to said first flip-flop for holding and updating a value of the shift-in test data ~~the output AC boundary scan cell~~;

an XOR logic gate connected to said second flip-flop for generating an AC ~~the~~ signal based on a reference clock signal and the value held in said second flip-flop, the AC signal having a first phase if a first value is held in said second flip-flop, and having a second phase if a second value is held in said second flip-flop; and

a multiplexor for selectively outputting the AC signal based on a mode signal ~~sending the signal~~.

24. (Currently Amended) An input AC boundary scan cell (BSC), comprising:

a first flip-flop having a data input for receiving an input signal, a clock input connected to a *refClk* line, and a first flip-flop output, the input signal being an AC signal if said BSC is in an AC JTAG mode and a DC signal if said BSC is a non-AC JTAG mode, the first flip-flop output indicating a captured phase of the AC signal if the input signal is the AC signal;

a first multiplexer having a first input, a select input connected to a *syncPulse* ~~syncPulse~~ line, a second input connected to said first flip-flop output, and a first multiplexer output, a sync pulse signal on the *syncPulse* line having an initial pulse;

a second flip-flop having a data input connected to said first multiplexer output, a clock input connected to a *refClk* line, and a second flip-flop output feedback to said first input of said first multiplexer, said second flip-flop adapted to capture a default phase of the AC signal in the AC-JTAG mode when the sync pulse signal has the initial pulse, the second flip-flop output indicating the default phase;

an XOR logic gate having a first input connected to said second flip-flop output, a second input connected to said first flip-flop output, and an XOR logic gate output, the

XOR logic gate output having a first level if the first flip-flop output and the second flip-flop output match, and having a second level if the first flip-flop output and the second flip-flop output do not match;

a second multiplexer having a first input connected to said first flip-flop output, a select input connected to ~~and~~ an *acjtagMode* line, a second input connected to said XOR logic gate output, and a second multiplexer output;

a third multiplexer having a first input connected to a *bscanShiftIn* line, a select input connected to ~~and~~ a *ShiftBscan2Edge* line, a second input connected to said second multiplexer output, and a third multiplexer output; and

a third flip-flop having a first input connected to said third multiplexer output, a second input connected to a *clockBscan* line, and a third flip-flop output connected to a *bscanShiftOut* line.

25. (Currently Amended) An input AC coupled boundary scan cell (BSC) for receiving a signal, said BSC comprising:

a sampling flip-flop for sampling an input signal in accordance with ~~respect to~~ a reference clock, the input signal being an AC signal if said BSC is in an AC JTAG mode, the sampling flip-flop adapted to capture and output a phase of the AC signal if the input signal is the AC signal;

a feedback flip-flop connected to said sampling flip-flop, said feedback flip-flop adapted to capture a default phase of the AC signal when a sync pulse signal has an initial pulse, an output of said feedback flip-flop indicating the default phase ~~for controlling the signal~~; and

an XOR logic ~~a multiplexer~~ connected to the output of said sampling flip-flop and the output of said feedback flip-flop, an output of said XOR logic gate output having a first level if the output of said sampling flip-flop and the output of said feedback flip-flop match, and having a second level if the output of said sampling flip-flop and the output of said feedback flip-flop do not match ~~for decoding the signal~~.

26. (Original) The input AC coupled boundary scan cell according to claim 25 further comprising a shifting out flip-flop connected to said multiplexer for processing the signal.

27. (New) The method according to claim 1, wherein the second phase is an inverted phase of the first phase.

28. (New) The method according to claim 1, wherein the sync pulse signal is generated based on the reset signal when a mode select signal is active high.

29. (New) The method according to claim 1, wherein the phase decode signal has a first value if the captured phase of the AC signal matches the default phase, and a second value if the captured phase of the AC signal does not match the default phase.

30. (New) The method according to claim 1, wherein said capturing the default phase comprising:

capturing a signal level of the AC signal using the reference clock in response to the sync pulse signal; and

setting the captured signal level as a default phase signal level.

31. (New) The method according to claim 30, wherein said capturing the phase of the AC signal comprising:

capturing a signal level of the AC signal using the reference clock.

32. (New) The method according to claim 31, wherein the phase decode signal have a first value if the captured signal level of the AC signal has the default phase signal level, and a second value if the captured signal level of the AC signal does not have the default phase signal level.

33. (New) The method according to claim 3, wherein the default value is zero.

34. (New) The system according to claim 8, wherein the second phase is an inverted phase of the first phase.

35. (New) The system according to claim 8, wherein the sync pulse signal is generated based on the reset signal when a mode select signal is active high.

36. (New) The system according to claim 8, wherein the phase decode signal has a first value if the captured phase of the AC signal matches the default phase, and a second value if the captured phase of the AC signal does not match the default phase.

37. (New) The system according to claim 8, wherein said means for capturing the default phase comprising:

means for capturing a signal level of the AC signal using the reference clock in response to the sync pulse signal; and

means for setting the captured signal level as a default phase signal level.

38. (New) The system according to claim 37, wherein said means for capturing the phase of the AC signal comprising:

means for capturing a signal level of the AC signal using the reference clock.

39. (New) The system according to claim 38, wherein the phase decode signal have a first value if the captured signal level of the AC signal has the default phase signal level, and a second value if the captured signal level of the AC signal does not have the default phase signal level.

40. (New) The system according to claim 10, wherein the default value is zero.

41. (New) The program storage device according to claim 15, wherein the second phase is an inverted phase of the first phase.

42. (New) The program storage device according to claim 15, wherein the sync pulse signal is generated based on the reset signal when a mode select signal is active high.

43. (New) The program storage device according to claim 15, wherein the phase decode signal has a first value if the captured phase of the AC signal matches the default phase, and a second value if the captured phase of the AC signal does not match the default phase.

44. (New) The program storage device according to claim 15, wherein said capturing the default phase comprising:

capturing a signal level of the AC signal using the reference clock in response to the sync pulse signal; and

setting the captured signal level as a default phase signal level.

45. (New) The program storage device according to claim 44, wherein said capturing the phase of the AC signal comprising:

capturing a signal level of the AC signal using the reference clock.

46. (New) The program storage device according to claim 45, wherein the phase decode signal have a first value if the captured signal level of the AC signal has the default phase signal level, and a second value if the captured signal level of the AC signal does not have the default phase signal level.

47. (New) The program storage device according to claim 17, wherein the default value is zero.

48. (New) The output AC boundary scan cell according to claim 22, wherein said multiplexer outputs a DC test data input signal from the *fromCore* line if the mode signal on the *selctJtagOut* line indicates non-AC JTAG mode.

49. (New) The output AC boundary scan cell according to claim 23, wherein said multiplexer outputs a DC test data input signal supplied from a first input if the mode signal indicates a non-AC JTAG mode, and outputs the AC signal supplied from a second input if the mode signal indicates the AC JTAG mode.

50. (New) The input AC coupled boundary scan cell according to claim 25, further comprising:

a multiplexer coupled to said sampling flip-flop and said XOR logic, said multiplexer adapted to selectively outputting one of the output of said sampling flip-flop and the output of said XOR logic based on a mode select signal.